WHAT IS CLAIMED IS:

1. An arbitration system for a network switch element, comprising:

an encoder for encoding a plurality of inputs into address information associated with a storage structure, said inputs corresponding to control signals generated by a plurality of entities associated with a cross-connect matrix of said network switch element, wherein said entities are operable to establish a set of connections through said cross-connect matrix for transporting data from said network switch element's ingress side to its egress side;

said storage structure including a plurality of fields for storing pre-computed arbitration results based on a select arbiter scheme employed in a particular scheduling mechanism for transporting said data, wherein each arbitration result corresponds to at least a particular input combination; and

a decoder for decoding a selected arbitration result into an identity associated with a corresponding entity.

2. The arbitration system for a network switch element as set forth in claim 1, wherein said storage structure comprises a look-up table.

3. The arbitration system for a network switch element as set forth in claim 1, wherein said storage structure is realized in a read-only memory (ROM).

4. The arbitration system for a network switch element as set forth in claim 1, wherein said storage structure is realized in an electrically programmable read-only memory (EPROM).

5. The arbitration system for a network switch element as set forth in claim 1, wherein said storage structure is realized in a dynamic random access memory (DRAM).

6. The arbitration system for a network switch element as set forth in claim 1, wherein said storage structure is realized in a static random access memory (SRAM).

7. The arbitration system for a network switch element as set forth in claim 1, wherein said storage structure is realized in a Flash memory.

8. The arbitration system for a network switch element as set forth in claim 1, wherein said storage structure is realized in a field-programmable gate array (FPGA).

9. The arbitration system for a network switch element as set forth in claim 1, wherein said storage structure is realized in a application-specific integrated circuit (ASIC).

10. The arbitration system for a network switch element as set forth in claim 1, wherein said select arbiter scheme includes at least one flexible ring arbiter.

11. The arbitration system for a network switch element as set forth in claim 1, wherein said select arbiter scheme includes at least one binary tree arbiter (BTA).

12. The arbitration system for a network switch element as set forth in claim 1, wherein said select arbiter scheme includes at least one round-robin arbiter (RRA).

13. The arbitration system for a network switch element as set forth in claim 1, wherein said select arbiter scheme includes at least one fixed priority arbiter.

14. The arbitration system for a network switch element as set forth in claim 1, wherein said select arbiter scheme is implemented at said network switch element's ingress side.

15. The arbitration system for a network switch element as set forth in claim 1, wherein said select arbiter scheme is implemented at said network switch element's egress side.

16. The arbitration system for a network switch element as set forth in claim 1, wherein said arbiter scheme is implemented as at least one of a request arbiter, a grant arbiter and an accept arbiter.

17. The arbitration system for a network switch element as set forth in claim 1, wherein said arbiter scheme is implemented as part of a Request-Grant-Accept (RGA) iteration strategy associated with said particular scheduling mechanism.

18. The arbitration system for a network switch element as set forth in claim 1, wherein said arbiter scheme is implemented as part of a Request-Grant (RG) iteration strategy associated with said particular scheduling mechanism.

19. The arbitration system for a network switch element as set forth in claim 1, wherein said encoder is operable to encode prior state information associated with select arbiter scheme into a portion of said address information, wherein said prior state information is operable to be updated by said select arbiter scheme in a predetermined manner.

20. An arbitration methodology for a network switch element, comprising the steps:

encoding a plurality of inputs into address information associated with a storage structure, said inputs corresponding to control signals generated by a plurality of entities associated with a cross-connect matrix of said network switch element, wherein said entities are operable to establish a set of connections through said cross-connect matrix for transporting data from said network switch element's ingress side to its egress side;

storing pre-computed arbitration results in a plurality of fields associated with said storage structure, wherein said arbitration results are based on a select arbiter scheme employed in a particular scheduling mechanism for transporting said data, each arbitration result corresponding to at least a particular input combination;

responsive to a particular input combination in an arbitration iteration, obtaining a selected arbitration result from said storage structure; and

decoding said selected arbitration result into an identity associated with a corresponding selected entity for said arbitration iteration.

21. The arbitration methodology for a network switch element as set forth in claim 20, further comprising the steps:

updating prior state information associated with said select arbiter scheme in a predetermined manner based on said arbitration result obtained in an arbitration iteration; and

utilizing said updated state information as at least a portion of said address information for a next arbitration iteration.

22. The arbitration methodology for a network switch element as set forth in claim 20, wherein said pre-computed arbitration results are stored in a look-up table (LUT).

23. The arbitration methodology for a network switch element as set forth in claim 20, wherein said pre-computed arbitration results are stored in a storage structure selected from the group consisting of a read-only memory (ROM) structure, an electrically programmable read-only memory (EPROM) structure, a dynamic random access memory (DRAM) structure, a static random access memory (SRAM) structure, a Flash memory structure, a field-programmable gate array (FPGA) and an application-specific integrated circuit (ASIC).

24. The arbitration methodology for a network switch element as set forth in claim 20, wherein said select arbiter scheme includes at least one flexible ring arbiter.

25. The arbitration methodology for a network switch element as set forth in claim 20, wherein said select arbiter scheme includes at least one binary tree arbiter (BTA).

26. The arbitration methodology for a network switch element as set forth in claim 20, wherein said select arbiter scheme includes at least one round-robin arbiter (RRA).

27. The arbitration methodology for a network switch element as set forth in claim 20, wherein said select arbiter scheme includes at least one fixed priority arbiter.

28. The arbitration methodology for a network switch element as set forth in claim 20, wherein said select arbiter scheme is implemented at said network switch element's ingress side.

29. The arbitration methodology for a network switch element as set forth in claim 20, wherein said select arbiter scheme is implemented at said network switch element's egress side.

30. The arbitration methodology for a network switch element as set forth in claim 20, wherein said arbiter scheme is implemented as at least one of a request arbiter, a grant arbiter and an accept arbiter.

31. The arbitration methodology for a network switch element as set forth in claim 20, wherein said arbiter scheme is implemented as part of a Request-Grant-Accept (RGA) iteration strategy associated with said particular scheduling mechanism.

32. The arbitration methodology for a network switch element as set forth in claim 20, wherein said arbiter scheme is implemented as part of a Request-Grant (RG) iteration strategy associated with said particular scheduling mechanism.